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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,807	02/25/2004	Hui-Mei Chen	085027-0106	3341
89518	7590	09/02/2010	EXAMINER	
McDermott Will & Emery LLP 11682 El Camino Real Suite 400 San Diego, CA 92130			AU, BAC H	
			ART UNIT	PAPER NUMBER
			2822	
			NOTIFICATION DATE	DELIVERY MODE
			09/02/2010	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

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## **DETAILED ACTION**

### ***Response to Amendment***

1. Applicant's amendment dated July 12, 2010, in which claims 15, 27, 35-37, 39, and 41 were amended, has been entered.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 15, 27, 35-39, and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 15, 27, and 37, the limitation "... and prior to wafer testing of said semiconductor wafer..." is vague and ambiguous. It is not clear whether a wafer testing step is a required limitation.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara (U.S. Pub. 2003/0127747) in view of Hikita (U.S. Pub. 2003/0146518) and Broz (U.S. Pub. 2004/0115934).

Regarding claim 15, Kajiwara [Fig.1] discloses a method for fabricating a circuit component, comprising:

providing a semiconductor wafer [1], a metal pad [4] over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer [5] on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said metal pad and first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure [7] over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect [Kajiwara, in Figs.1,6,7, discloses metallization structures [7, 103, and 123/124] that are in the opening of the passivation layer [5,102], over the passivation layer 122, and directly on the passivation layer 122]; and

after said providing said exposed metallization structure, performing a sputter etching process with an argon gas [Para.39].

Kajiwara fails to explicitly disclose wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar

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top surface of said metal bump. However, Hikita [Fig.1] discloses a method for fabricating a circuit component wherein said metal bump [3] has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. Hikita discloses and makes obvious the suitable alternatives of various shapes of metal bumps. Because both references teach methods of forming metal bumps for external electrical connection in a semiconductor device, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of having the suitable bump design for the required device manufacturing process.

Kajiwara [Para.39] discloses surface cleaning a circuit component by sputter etching, but fails to explicitly disclose performing the sputter etching prior to wafer testing of said semiconductor wafer. However, Broz [Paras.2-3,7,16,19-21] discloses a method for fabricating a circuit component, comprising performing a sputter etching prior to wafer testing of said semiconductor wafer. Because both references teach methods of surface cleaning a circuit component by sputter etching in forming metal bumps for external electrical connection in a semiconductor device, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of effectively removing contaminants and residues to facilitate probing during testing as well as to improve device performance by lowering contact resistance in subsequent processing steps [Broz; paras.2-3,7].

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara (U.S. Pub. 2003/0127747) in view of Hikita (U.S. Pub. 2003/0146518) and Broz (U.S. Pub. 2004/0115934), as applied to claim 15, and further in view of Dass (U.S. Pat. 6162652).

Regarding claim 35, Kajiwara discloses performing said sputter etching process, but fails to disclose wherein after said performing said sputter etching process, further comprising having a testing probe contact said metal bump. However, Dass [Fig.17] discloses wherein a method for fabricating a circuit component further comprising contacting said metal bump [150] with a testing probe [160]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Dass into the method of Kajiwara to include wherein a method for fabricating a circuit component further comprising contacting said metal bump with a testing probe. The ordinary artisan would have been motivated to modify Kajiwara in the manner set forth above for at least the purpose of performing in-process testing of the separate component before proceeding with subsequent packaging steps to avoid additional costs in the event the component is rejected [Dass; col.1 lines 11-25].

4. Claims 27 and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara (U.S. Pub. 2003/0127747) in view of Fan (U.S. Pat. 6956292), Hikita (U.S. Pub. 2003/0146518), and Broz (U.S. Pub. 2004/0115934).

Regarding claims 27 and 37-38, Kajiware [Fig.1] discloses a method for fabricating a circuit component, comprising:

providing a semiconductor wafer [1], a metal pad [4] over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer [5] over said semiconductor wafer and on said second region, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure [7] over said semiconductor wafer, over said passivation layer; directly on said passivation layer; and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect [Kajiware, in Figs.1,6,7, discloses metallization structures [7, 103, and 123/124] that are in the opening of the passivation layer [5,102], over the passivation layer 122, and directly on the passivation layer 122].

Kajiware discloses after said providing said exposed metallization structure, performing a sputter etching process with an argon gas [Para.39]. Kajiware fails to explicitly disclose performing an ion milling process with an argon gas; with an inert gas. However, Fan [Col.5 lines 12-14] discloses performing an ion milling process with an argon gas; with an inert gas. Fan discloses and makes obvious that sputter etching and ion milling are suitable alternative processes. Because both references teach methods

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of cleaning of metal surfaces with ions, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of having an effective method of cleaning metal surfaces, particularly metal bumps.

Kajiwara fails to explicitly disclose wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. However, Hikita [Fig.1] discloses a method for fabricating a circuit component wherein said metal bump [3] has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. Hikita discloses and makes obvious the suitable alternatives of various shapes of metal bumps. Because both references teach methods of forming metal bumps for external electrical connection in a semiconductor device, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of having the suitable bump design for the required device manufacturing process.

Kajiwara [Para.39] discloses surface cleaning a circuit component by sputter etching, but fails to explicitly disclose performing the sputter etching prior to wafer testing of said semiconductor wafer. However, Broz [Paras.2-3,7,19-21] discloses a method for fabricating a circuit component, comprising performing a sputter etching prior to wafer testing of said semiconductor wafer. Because both references teach methods of surface cleaning a circuit component by sputter etching in forming metal

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bumps for external electrical connection in a semiconductor device, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of effectively removing contaminants and residues to facilitate probing during testing as well as to improve device performance by lowering contact resistance in subsequent processing steps [Broz; paras.2-3,7].

Claims 36 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara (U.S. Pub. 2003/0127747) in view of Fan (U.S. Pat. 6956292), Hikita (U.S. Pub. 2003/0146518), and Broz (U.S. Pub. 2004/0115934), as applied to claims 27 and 37 above, and further in view of Dass (U.S. Pat. 6162652).

Regarding claims 36 and 41, the limitations of the claims were already addressed above in the treatment of claim 35.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara (U.S. Pub. 2003/0127747) in view of Fan (U.S. Pat. 6956292), Hikita (U.S. Pub. 2003/0146518), and Broz (U.S. Pub. 2004/0115934), as applied to claim 37 above, and further in view of Zhang (U.S. Pat. 6104461).

Regarding claim 39, Kajiwara and Fan disclose wherein said inert gas comprises an argon gas, but fails to disclose a helium gas. However, Zhang [Col.10 lines 63-65] discloses wherein said inert gas comprises a helium gas. Zhang makes it obvious that ion milling can be done with either argon or helium, which can be used as suitable alternatives in the ion milling process. Because all three references teach methods of

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sputtering or ion milling with an inert gas, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of having an effective method of etching or cleaning metal surfaces.

### ***Response to Arguments***

5. Applicant's arguments filed July 12, 2010 have been fully considered but they are not persuasive. Applicant asserts "Kajiwara's sputter etching process is therefore taught to be performed for flip-chip bonding to sputter etch an Au bump, but is not taught to be performed for testing. Even though Broz teaches that after performing a sputter etching process, a testing process can be performed in a wafer level process, (see, e.g., Broz, para. [0016], lines 7, 28 and 29), Broz's testing process is believed not to be applicable to Kajiwara's flip-chip bonding process because multiple steps in a wafer-level process, typically performed before a die sawing step, are not believed to be readily transferred to a flip-chip bonding process, typically performed after the die sawing step. Furthermore, the considerations of an apparatus or mechanism for testing a chip package formed after a die sawing step are significantly different from those for testing a wafer provided before the die sawing step". These assertions are not persuasive, as they are mere conjectures and are unsupported by facts. Applicant further asserts "combination of Broz's wafer-level testing process with Kajiwara's flip-chip configuration therefore would change the principle of operation of Broz's wafer-level testing process". This assertion is respectfully traversed. The principal of operation of Broz's wafer-level testing process is, in fact, very pertinent to flip-chip

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bonding [Broz, para.17 lines 1-3], and it is known that flip-chip bonding is routinely carried out on both wafer level and separated die level. The principal of contaminant removal as well as testing are indeed also transferable between wafer and separated die levels. The combination of Kajiwara and Broz is deemed proper as their combination was adequately presented and rationale/motivation for their combination was given.

Overall, Applicant's arguments are not persuasive, and the claims stand rejected.

### ***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bac H. Au whose telephone number is 571-272-8795. The examiner can normally be reached on Mon-Fri 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bac H Au/  
Examiner, Art Unit 2822

/Kevin M. Picardat/  
Primary Examiner, Art Unit 2822